



PATENT

AND TRADEMARK OFFICE IN THE UNITED STATES PATEN

Applicant:

Leonard Forbes et al.

Examiner: W. Mintel

Serial No.:

08/903,486

Group Art Unit: 2811

Filed:

July 29, 1997

Docket: 303.326US1

Title:

SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Applicants have included the fee of \$240.00 under 37 C.F.R. §§ 1.97(c) and 1.17(p). Please charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representatives at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on July 15, 1999.

07/21/1999 TLUU11 00000010 190743 08903486